

CCAA Equal MIL-PRF-55681/4/5



1. Capacitor characteristics and applications

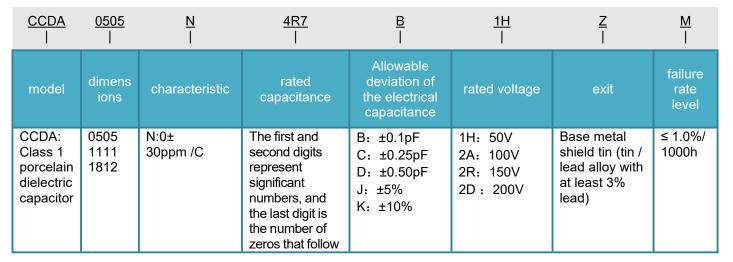
1.1 FEATURES

- Size specification serial, suitable for surface mounting elements of hybrid integrated circuit or printed circuit;
- It has the characteristics of low loss, high electrical capacity stability and high reliability;
- Suitable for all kinds of equipment in the high frequency circuit, amplification circuit;

1.2 Main performance indicators

- Temperature coefficient: NPO: 0 ± 30ppm /℃
- Capacitance drift: no more than ± 0.2% or ± 0.05 pF, take the larger
- Loss angle tangent: not exceeding 0. 15% at a frequency of 1 MHz / 1 KHz
- Insulation resistance (25℃): 100000M Ω
- Medium voltage resistance (test surge current does not exceed 50mA): 2.5 UR
- Operating temperature: -55~125 ℃

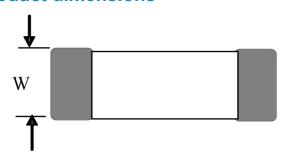


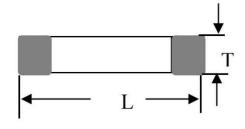






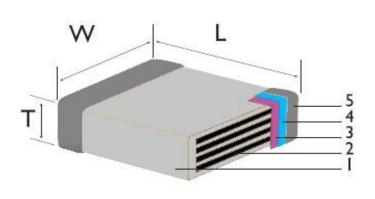
3. Product dimensions





mod	el	Dimensions (mm)						
The British system said			W	T _{max}				
0505	1212	$1.40 \begin{array}{c} +0.38 \\ -0.25 \end{array}$	1.40±0.38	1.45				
1111	2828	$2.79 \begin{array}{c} +0.51 \\ -0.25 \end{array}$	2.79±0.38	2.59				
1812	4532	4.50±0.40	3.20±0.30	3.10				

Note: Products that meet customer requirements can be designed according to the special requirements of customers.



order number	name
1	ceramic dielectric
2	inner electrode
3	External electrode
4	nickel dam
5	Lead tin layer





4. Capacity range

4.1 0505 Specification capacity value table

0505 specification and value table

Toleranc e code	Toleranc e (pF)	accur acy	Maximum direct current operating voltage (V)	Toleranc e code	Toleranc e (pF)	accuracy	Maxim um direct current operati ng voltage (V)	Toleranc e code	Toleranc e (pF)	accuracy	Maximum direct current operating voltage (V)	Capacity value code	Capacity value (pF)	accuracy	Maximum direct current operating voltage (V)		
0R2	0.2							9R1	9.1	B,C		510	51				
0R3	0.3	B ,C		1R9	1.9							560	56				
0R4	0.4			2R0	2			100	10			620	62				
				2R1	2.1			110	11			680	68				
				2R2	2.2			120	12			750	75		150		
0R5	0.5			2R4	2.4			130	13			820	82				
0R6	0.6			2R7	2.7			150	15			910	91				
0R7	0.7			3R0	3			160	16			101	100				
0R8	0.8			3R3	3.3		180	18					F,G,				
0R9	0.9			3R6	3.6	B,C,		200	20	F,G,	200						
1R0	1		200	3R9	3.9	D,0,	200	220	22	J,K,	200	111	110	J,K,			
1R1	1.1	B,C,		4R3	4.3			240	24	М		121	120	М	50		
1R2	1.2			4R7	4.7			270	27								
1R3	1.3	D				5R1	5.1			300	30						
1R4	1.4			5R6	5.6			330	33								
1R5	1.5			6R2	6.2			360	36								
1R6	1.6			6R8	6.8			390	39								
1R7	1.7			7R5	7.5			430	43								
1R8	1.8			8R2	8.2			470	47								





4.2 1111 Specification capacity value table

1111 Specification capacity value table

Tolerance code	Tolerance (pF)	accuracy	Maximum direct current operating voltage (V)	Tolerance code	Tolerance (pF)	accuracy	Maximum direct current operating voltage (V)		Tolerance (pF)	accuracy	Maximum direct current operating voltage (V)		Capacity value (pF)	accuracy	Maximum direct current operating voltage (V)
0R2	0.2			00.4	0.4			200	20		151	150	50		
0R3	0.3	B ,C		2R4	2.4							161	160		
0R4	0.4			2R7	2.7			220	22			181	180		
				3R0	3			240	24			201	200		
				3R3	3.3			270	27			221	220		200
0R5	0.5			3R6	3.6			300	30						
0R6	0.6			3R9	3.9			330	33			241	240		
0R7	0.7			4R3	4.3			360	36			271	270		
0R8	0.8			4R7	4.7	B,C,		390	39			301	300		150
0R9	0.9			5R1	5.1	D	D	430	43			331	330	-	130
1R0	1			5R6	5.6			470	47			361	360		
1R1	1.1			6R2	6.2			510	51			391	390		100
1R2	1.2			6R8	6.8		560	56	F,G,			F,G	F,G		
			200				200			J,K, M	200	431 430 471 470	430	,J,K, M	
1R3	1.3	B,C,		7R5	7.5			620	62	IVI			470	IVI	
1R4	1.4	D		8R2	8.2			680	68						
1R5	1.5			9R1	9.1			750	75						
1R6	1.6														
1R7	1.7			100	10			820	82						
1R8	1.8			110	11			910	91						50
1R9	1.9			120	12			101	100						
2R0	2			130	13	F,G,		111	110						
2R1	2.1			150	J,K	J,K,		121	120						
2R2	2.2					15 M		131	130						
				160											
				180	18										





4.3 1812 Specification capacity value table

1812 Specification value table

Tolerance code	Tolerance (pF)	accuracy	Maximum direct current operating voltage (V)	Tolerance code	Tolerance (pF)	accuracy	Maximum direct current operating voltage (V)	Tolerance code	Tolerance (pF)	accuracy	Maximum direct current operating voltage (V)		Capacity value (pF)	accuracy	Maximum direct current operating voltage (V)				
				4R3	4.3							241	240						
0R5	0.5			4R7	4.7			330	33			271	270						
0R6	0.6			5R1	5.1			360	36			301	300						
0R7	0.7			5R6	5.6			390	39			331	330						
0R8	0.8			6R2	6.2	B,C,D		430	43			361	360		200				
0R9	0.9			6R8	6.8	В,О,В		470	47			391	390						
1R0	1			7R5	7.5			510	51			431	430						
1R1	1.1			8R2	8.2			560	56			471	470						
1R2	1.2			9R1	9.1	.1						620	62						
1R3	1.3							680	68			511	510	F,G	150				
1R5	1.5			100	10			750	75	F,G,		561	560	,J,	.00				
1R6	1.6	B,C,D	200	110	11			200	820	82	J,K,	200	621	620	, с, К, М				
1R8	1.8			120	12				910	91	М		681	680					
2R0	2			130	13							101	100			751	750	141	100
2R1	2.1			150	15			111	110			821	820						
2R2	2.2			160	16	F,G,		121	120										
2R4	2.4			180	18	J,K,		131	130										
2R7	2.7			200	20	М		151	150			911	910						
3R0	3			220				161	160			102	1000						
3R3	3.3			240	24	22		181	180			112	1100		50				
3R6	3.6			270	27			201	200			122	1200						
3R9	3.9			300	30			221	220										
				550	55														





5. Technical requirements and test conditions

5.1 Conventional electrical performance

project		hnical fications	test method							
operating temperature range		∙ +125) ℃								
surface		gnificant efect	eyeballing							
Electrostatic	\/\/it	hin the	nominal capacity	Test frequency	test voltage	ambient ten	nperature			
capacity of Capacitance	specific	ation error	≤1000pF	1MHz (±10%)	(1.0±0.2)Vrms	(25±2	\°C			
Capacitanicc	16	ange	>1000pF	1KHz (±10%)	(1.0±0.2)VIIIIS	(2012) C			
loss tangent (DF)	Not at 1 l	equency is MHz / 1 KHz · 0. 15%		Test method: the	same as the "static elec	ctricity capacity"				
insulation resistance	≥100000M Ω		rated voltage	test voltage	testing time	Charge and discharge current	environment			
(I .R). Insulation			Ur <1000V	Ur	(60±5) sec	≤50mA	temperature (25±2)℃			
Resistance			Ur ≥1000V	1000V	(60±5) sec	≤50mA	Humidity was <75%			
Electric resistance	Media should not be broken down or damaged		rated voltage	test voltage	duration	Charge and discharge current				
strength of the medium (D .W .V).			All voltage	2.5Ur	5 Seconds	≤50mA				
			The following	temperature ord	ler, 30min after tempe	rature stability	(△ C to T 3)			
			step		temperature	(℃)				
Capacity temperature	0.00	(0.00)	T 1		25±2					
coefficient or temperature	C 0G :	: (0±30) m /℃	T 2	Low	er limit Category temp	erature (-55 ± 3)			
characteristics			Т3		25±2					
			T 4	Upp	er limit Category tempe	erature (125 ± 2)			
			T 1		25±2					
		No visible damage,	Absolve the capacitor in ethanol and rosin (25% weight) solution, remove the temperature at (80∼120) ℃ (10-30) seconds, and soak the solder solution.							
Solder ability	surface	tin rate of	Tin immersion	temperature: (24	5 ± 2) $^{\circ}\mathrm{C}$; tin immersior	n speed: (25 ± 0.	25) mm / sec			
		95%		Tin imi	mersion time: (5 ± 0.5)	sec				

remarks:

When testing the dielectric power resistance strength of the capacitor, in order to eliminate the influence of the external environment, when the test voltage exceeds 2000 Vdc, then the capacitor should be soaked in insulating oil for testing.





5.2 Quality consistency test

Quality consistency test is A group A test, consisting of the following table and performed in the order shown. Equal MIL-PRF-55681/4/5

divide into groups	inspecting item	Requires the chapter number	Test method chapter number	sampling plan
A divide into groups	Voltage treatment	3.8 in ZZR-Q / CT 20003-2018	4.5.3 in GJB 192B- 2011	100%
A divide into groups	Insulation resistance (125℃)	3.11 in ZZR-Q / CT 20003- 2018	4.5.6 in GJB 192B- 2011	In accordance with GJB 192B-2011 Table 6
A divide into groups	Visual and mechanical inspection	3.3 in ZZR-Q / CT 20003- 2018, .4.1 3, 3.28, 3.29	4.5.2 in GJB 192B- 2011	In accordance with GJB 192B-2011 Table 6
A divide into groups	solder ability	3.15 in ZZR-Q / CT 20003- 2018	4.4.2 in GJB 192B- 2011	13 samples, and 0 failed

6.2.1 A1 group ——, voltage treatment

100% test, requirements: when appropriate, can select voltage processing screening.

Test temperature: 125_0^{+4} °C;

Test time:96₀⁺⁴hour; Applied voltage: 2U_R

6.2.2 A2 block —— Insulation Resistance (125℃)

Sampling test according to the requirements in Table 6 in GJB 192B-2011,

Test temperature: 125₀4°C;

test voltage U_C : $U_C = U_R (U_R < 1000V)$; Applied voltage time: (60 ± 5) seconds.

6.2.3 A3 group —— appearance and mechanical inspection

Sampling test according to the requirements in Table 6 in GJB 192B-2011, The size suitable for the gauge inspection shall be inspected;

Visual inspection of the sheet capacitor under a microscope (10 times magnification): No cracks and cracks, layering, and electrode exposure are allowed on the surface of the capacitor.

6.2.4 A4 grouping —— soldability

Draw 5 products from each batch;

Test conditions: the lead end of the capacitor continues in the welding tin groove of (245 \pm 2) $^{\circ}$ C (5 \pm 0.5) S;

Requirements: After testing, perform a visual inspection with a 10 x magnification lens. The surface of the lead end should be 95% evenly stained with tin, tin layer continuous. The remaining 5% allows only very small pinholes and no defects with solder immersion, but should not be concentrated in one area.





6. Notes for use

Notes for MLCC

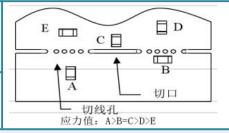
1. Notes before use:

The MLCC chip may be damaged under the harsh working environment or the external mechanical overpressure described in the relevant instructions in this admission letter, so first considering the relevant conditions in this admission letter.

2. The recommended layout

of the PC board design

- 2.1 The amount of solder used will affect the ability of the chip to resist mechanical stress, which may lead to the breakage or cracking of MLCC. Therefore, when designing the substrate, we must carefully consider the size and configuration of the welding pad, which has a decisive role in the amount of the solder composed of the substrate.
- 2.2 When designing the position of the pad and SMD MLCC, the stress shall be reduced to the lowest point, and the MLCC shall be installed in the least affected position on the PC plate.



3. Automatic installation should consider the problems

If the suction tube drops beyond the minimum limit, it will produce excessive pressure on the MLCC, which will cause the MLCC rupture. When lowering the tube, pay attention to the following points:

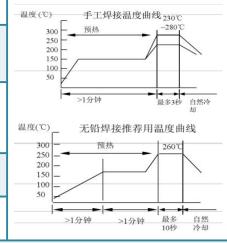
- 3.1 After correcting the deviation of the PC plate, the low limit of the suction tube should be adjusted to the surface horizontal position of the PC plate.
- 3.2 The suction pressure shall be adjusted between 1 and 3N.
- 3.3 In order to reduce the deformation degree of the PC plate caused by the impact force of the suction, the support nail shall be placed under the PC plate.

4. Welding

4.1 MLCC is a combination of ceramic and metal. As a ceramic body, especially the large size ceramic body, its thermoplasticity is poor, the response to heat is relatively slow, by the cold and hot, the ceramic body is easy to crack. It is recommended to conduct continuous preheating for more than 1 minute before welding.

The interior of the 4.2 MLCC is a metal electrode, which is very thermoplastic and responds responsive to heat. Therefore, in the case of heat, the metal part and the ceramic part must have a certain degree of inconsistent expansion, resulting in internal stress, easy to cause porcelain cracking. It is recommended to conduct continuous preheating for more than 1 minute before welding.

4.3 For manual welding, the maximum diameter of the tip with constant temperature iron is 1.0mm and the maximum power is 25 watts; the iron cannot directly touch the MLCC element.



5. Cleaning

- 5.1 The temperature difference between the components and the cleaning process shall not be greater than 100℃.
- 5.2 In the case of ultrasonic cleaning, if the output power is too large, the PC plate will withstand excessive vibration, which will cause the MLCC or welding point to crack, or reduce the strength of the end electrode. Therefore, special attention should be paid to the following points:

Ultrasonic output: less than 20W / L; ultrasonic frequency: less than 40 KHz; ultrasonic cleaning time: 5 minutes or less

6. Cut the PC plate

- 6.1 After installing the MLCC and other components, note that any force should be applied to the PC board. MLCC cannot tolerate excess
- 6.2 The segmentation of the board cannot be divided by hand, and appropriate equipment should be used.

7. Storage method

To maintain the weldability of the end electrodes and to keep the packaging materials in good condition, the recommended storage conditions are as follows:

Storage temperature: (5-40) °C; storage relative humidity: (20-70)% RH

The MLCC end weldability decreases over time even when stored under ideal storage conditions, so the MLCC should be used within 6 months from the date of shipment.







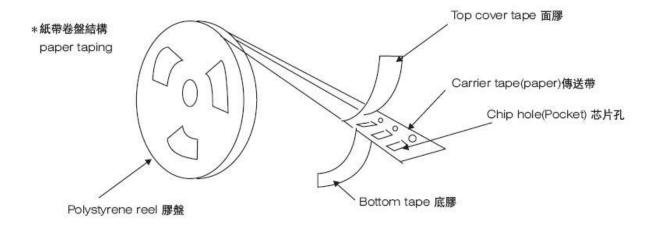
7. Product packaging

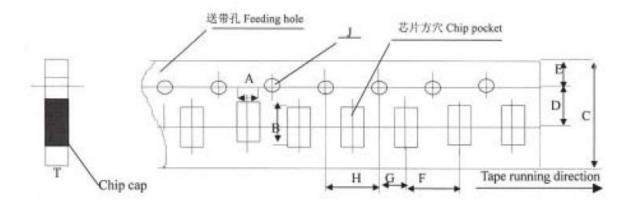
7.1 bags in bulk

specifications	bulk	remarks
0505	5000	
1111	2000	Packaging form and quantity can be determined according to the customer's requirements
1812	50	. 5 42 301.10

7.2 Paper tape packaging

7.2.1Paper tape coil structure





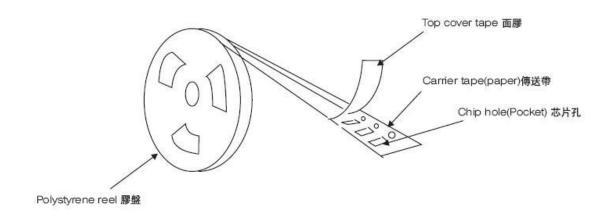


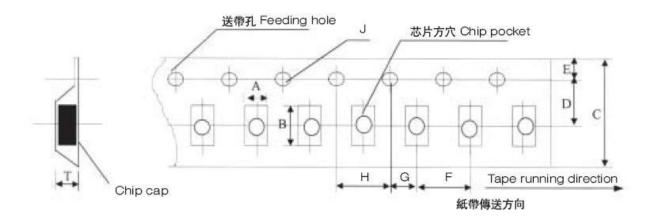


7.3 Plastic tape packaging

7.3.1 Plastic tape coil structure

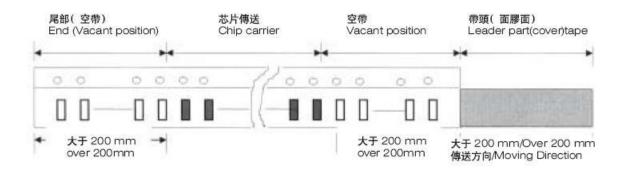
*塑膠卷盤結構 embossed taping





7.4 Front and rear structure of the conveyor belt

*傳送帶的前后結構 Structure of leader part and end part of the carrier paper

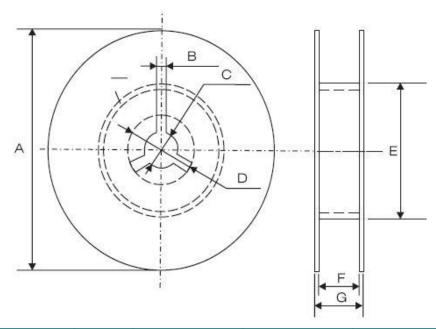






7.5 Reel dimensions

*卷盤尺寸 Reel Dimensions (unit:mm)



А	В	С	D	Е	F	G
Ф 178.00±2.00	3.00	Ф13.00±0.50	Ф21.00±0.80	Φ 50.00 or greater	10.00±1.50	12Max
Ф 330.00±2.00	3.00	Ф13.00±0.50	Ф21.00±0.80	Φ 50.00 or greater	10.00±1.50	12Max

7.6 Ribbon preparation method

- 8.6.1 The belt of the packaging capacitor is wound clockwise. When the belt is pulled from the top to the down direction, the transfer hole is on the right side of the belt.
- 8.6.2 For the front end of the strip, leave at least 5 spaced strips.
- .38.6 When compiling the belt, the lead belt part or blank part must be reserved according to the figure below.
- 8.6.4 The number of product errors in the installation of the disk must be less than 0. 1% of the number or 1 per disk, discontinuous errors.
- 8.6.5 The upper and lower tape shall not exceed the edge of the tape and shall not block the transfer hole.
- 8.6.6 The cumulative error of the transmission hole is 10 spacing: \pm 0.3 mm.
- 8.6.7 The stripping moment of the upper tape shall be within 0.1 to 0.7 Newton as shown in the following below.

